Course Specifications

From the academic year 2012-2013 up to and including the academic year 2013-2014

Digital Building Blocks (E031341)

<table>
<thead>
<tr>
<th>Course size</th>
<th>(nominal values; actual values may depend on programme)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Credits</td>
<td>6.0</td>
</tr>
<tr>
<td>Study time</td>
<td>180.0 h</td>
</tr>
<tr>
<td>Contact hrs</td>
<td>52.5 h</td>
</tr>
</tbody>
</table>

Course offerings and teaching methods in academic year 2013-2014

<table>
<thead>
<tr>
<th>A (semester 2)</th>
<th>practicum</th>
<th>20.0 h</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>lecture</td>
<td>35.0 h</td>
</tr>
<tr>
<td></td>
<td>self-reliant study activities</td>
<td>10.0 h</td>
</tr>
</tbody>
</table>

Lecturers in academic year 2013-2014

- Dambre, Joni (TW06) lecturer-in-charge
- Doutreligne, Jan (TW06) co-lecturer

Offered in the following programmes in 2013-2014

| Master of Science in Electrical Engineering | 6 | A |
| Master of Science in Computer Science Engineering (main subject Embedded Systems) | 6 | A |
| Master of Science in Electrical Engineering (main subject Electronic Circuits and Systems) | 6 | A |

Teaching languages

Dutch

Keywords

digital CMOS circuits, power dissipation, speed, deep-submicron

Level

specialist

Position of the course

This course aims at acquiring knowledge and expertise in the design of good digital CMOS circuits that can be used as building blocks in digital system design. The circuits are studied at circuit level and logic level, and important metrics like area, speed and dissipation are addressed. The lab work involves the effective design of circuits and the analysis of their properties using modern CAD software. To get acquainted with scientific literature, an advanced digital circuit design topic is studied in small groups and the results are presented to the class.

Contents

- Introduction: metrics for digital circuits
- CMOS Semiconductor components: semiconductor properties, the CMOS diode, the MOSFET transistor
- Post-CMOS technologies
- Integrated wires: properties, design
- Combinational CMOS Circuits: the CMOS Inverter, static circuits, dynamic circuits
- Sequential CMOS Circuits: static circuits, dynamic circuits
- Timing and Clock Distribution: timing and synchronisation of sequential circuits, synchronous circuits
- Special Building Blocks: arithmetic building blocks, memories
- Standard-cell design flow: optimization, technology mapping, automated physical design (placement, routing)
- Testing and testability

(Approved)
• Design, layout and characterize simple digital building blocks (logic gates, flipflops)
• Advanced topics in research and development: topics depending on recent
  evolutions and class preferences

**Initial competences**

Required prior knowledge: linear electrical networks (charge, current, potential, voltage,
  power, resistance, capacitance, induction, rc-networks), basic knowledge about digital
  gates (AND, OR, INVERTOR, ...), elementary logic synthesis, , combinational and
  sequential digital circuits, basic knowledge of computer architecture (components of a
  processor, memory hierarchy, ALU-components: binary addition, multiplication, ...),
  switch model for the MOSFET transistor, physical meaning of the term 'semiconductor',
  notions of VLSI-technology (physical structure of a MOSFET, most common process
  steps)

At Ghent University, this can be obtained by following:
  - the Bachelor electrical engineering courses: Electrical networks, Digital electronics,
    Computer architecture;
  - or the Bachelor informatics courses: Introductory electronics, Computer architecture;

**Final competences**

• Thoroughly understand the operation of nanoscale MOSFET transistors.
• Estimate the impact on the performance of integrated digital gates of scaling and of
  physical, environmental and design parameters.
• Describe the technological evolutions regarding digital circuits and elaborate on their
  consequences.
• Know how interconnections influence the performance of integrated digital circuits
  and how this impact evolves with scaling.
• Know the structure and properties of the most common families of digital gates and
  memory cells.
• Analyse complex digital gate circuits both theoretically and by simulation.
• Understand the principles of fundamental approaches to technology-dependent
  optimization at the logic level and apply these techniques to simple examples.
• Explain the problem of testing and testability and know some approaches to test
  pattern generation.
• Grasp the complexity of optimization problems such as technology mapping,
  placement and routing in a standarc cell design flow and know the most common
  approaches to these problems.
• Design the circuit for complex gates in complementary static CMOS under given
  boundary conditions.
• Perform lay-out for simple gates and analyse the result using modern CAD software.

**Conditions for credit contract**

Access to this course unit via a credit contract is determined after successful competences
  assessment

**Conditions for exam contract**

This course unit cannot be taken via an exam contract

**Teaching methods**

Lecture, practicum, self-reliant study activities

**Extra Information on the teaching methods**

**Learning materials and price**

Presentation material (dutch); textbook J. Rabaey, A. Chandrakasan, B. Nikolic: "Digital
  mandatory for non Dutch speaking students)

**References**

• J. Rabaey, A. Chandrakasan, B. Nikolic: "Digital Integrated Circuits", Prentice-Hall,

(Approved)
Course content-related study coaching
Coaching of lab sessions and literature study; thematic online discussion forums for questions; individual coaching on request before or after classes or by appointment.

Evaluation methods
end-of-term evaluation and continuous assessment

Examination methods in case of periodic evaluation during the first examination period
Oral examination

Examination methods in case of periodic evaluation during the second examination period
Oral examination

Examination methods in case of permanent evaluation
Participation, assignment, skills test, peer assessment, report

Possibilities of retake in case of permanent evaluation
examination during the second examination period is not possible

Extra Information on the examination methods
During semester: graded lab sessions and lab reports; graded project (including peer-evaluation).
Frequency: 3 lab exercises of multiple sessions each with written report + a study project with presentation.

Calculation of the examination mark
Special conditions: Lab work (including project) and exam each account for 50% of total score, but in order to succeed, a score of at least 9/20 must be attained on each part; scores below 9/20 on either part can not be compensated. Project and lab work do not count for second session: there is only a single exam to evaluate whether the required competences have been attained (if you failed for the evaluation during the semester, an alternative assignment will be part of this exam).

Facilities for Working Students

Addendum

(Approved)